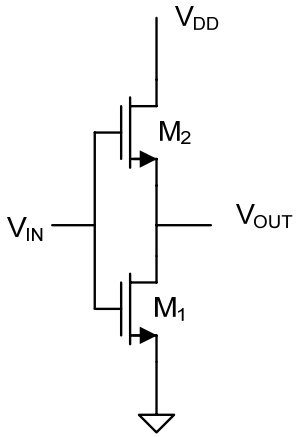
EE 434

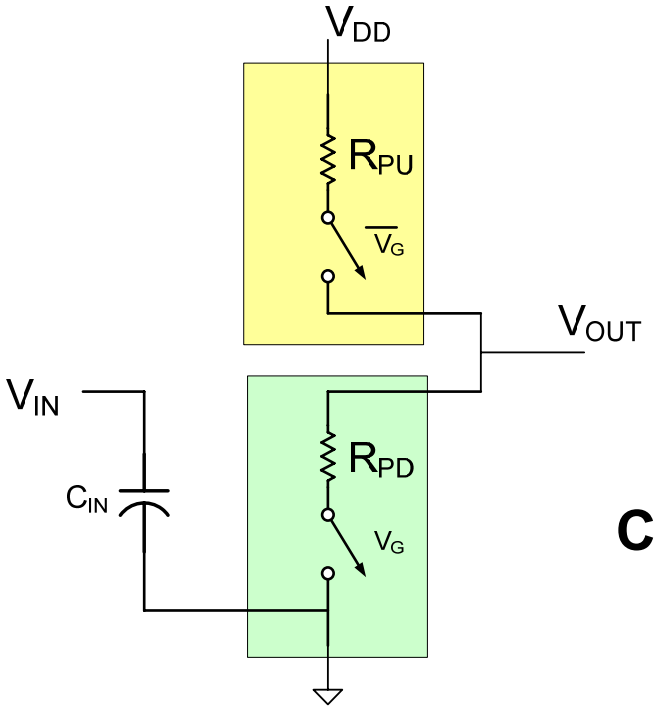
Lecture 35

Device Sizing

Propagation Delay in Logic Circuits

Propagation Delay in Static CMOS Family





$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX}(W_1 L_1 + W_2 L_2)$$

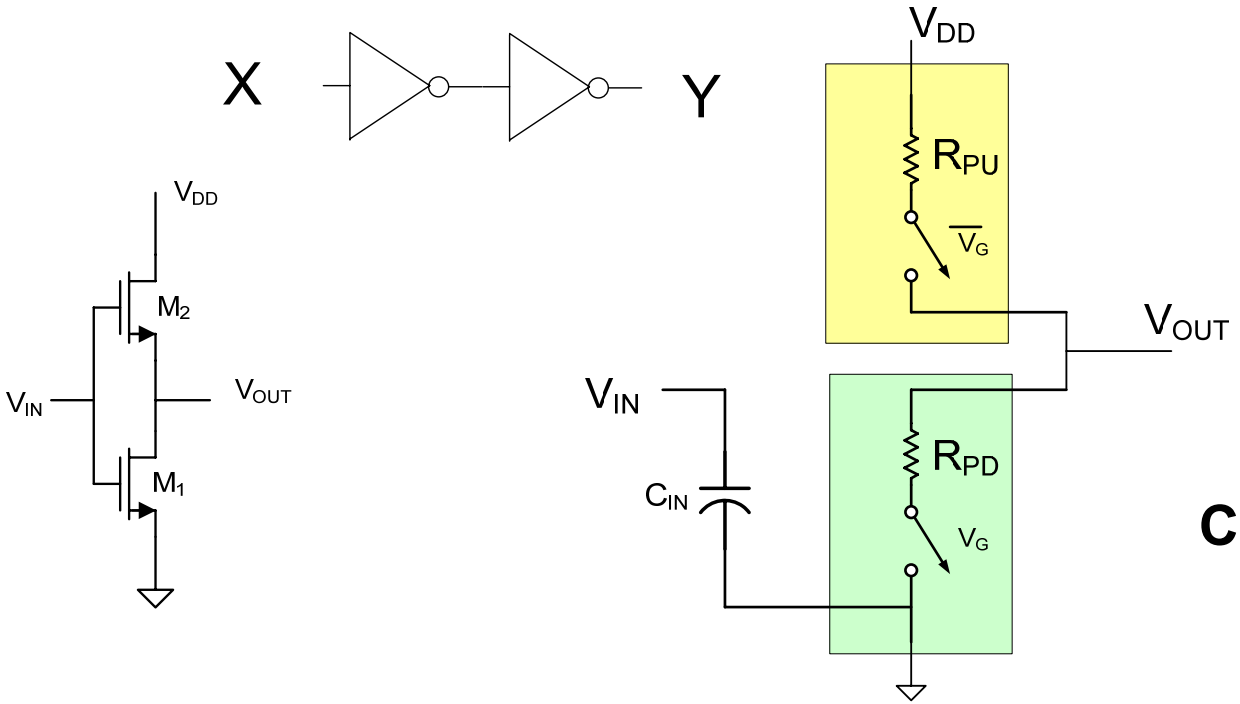
If $u_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=4\ fF\mu^{-2}$, $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN,}$ $L_{MIN}=0.5\mu$ and $V_{DD}=5V$

$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\Omega$$

$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\Omega$$

$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L_{MIN}^2 = 2fF$$

Propagation Delay in Static CMOS Family



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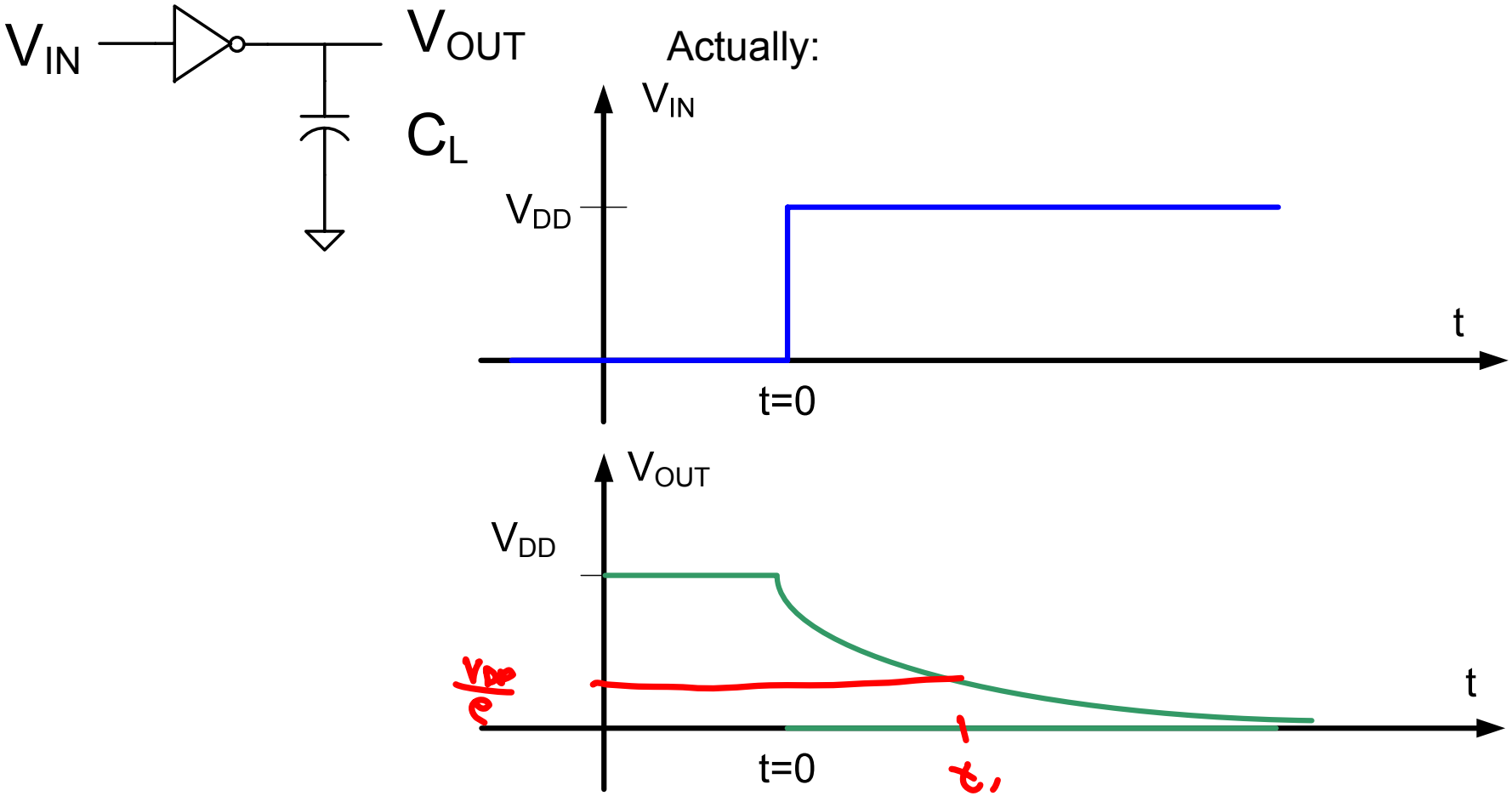
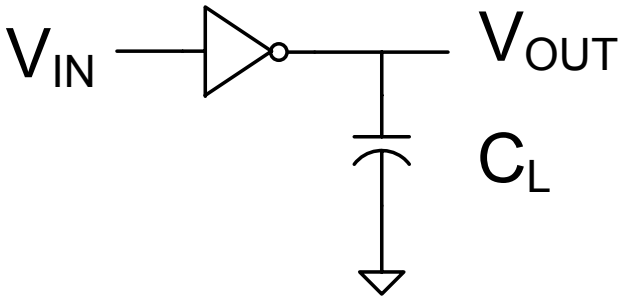
Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}



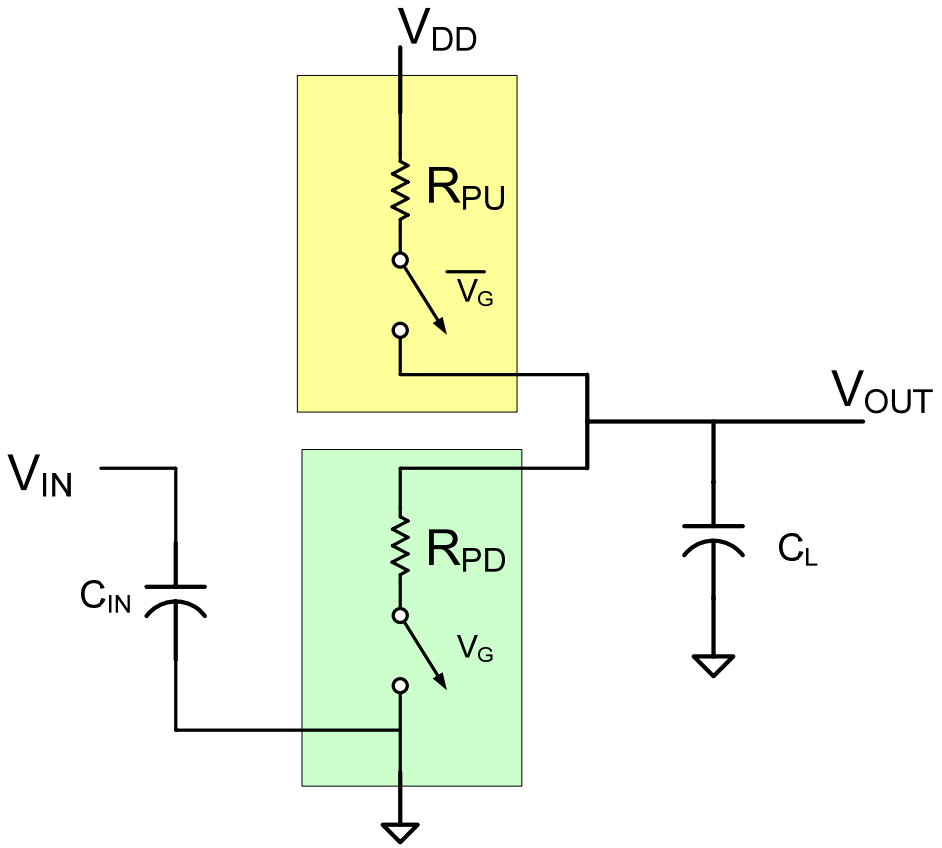
What is the transition time t_{HL} ?

Propagation Delay in Static CMOS Family



$t_{HL} = R_{PD} C_L$

$t_{LH} = R_{PU} C_L$



Propagation Delay in Static CMOS Family

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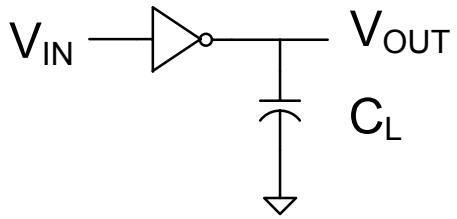
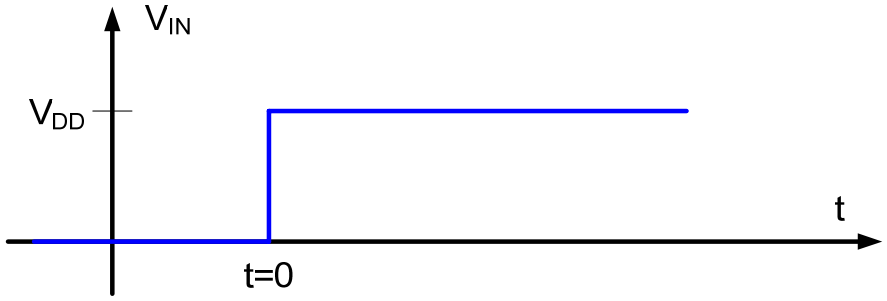
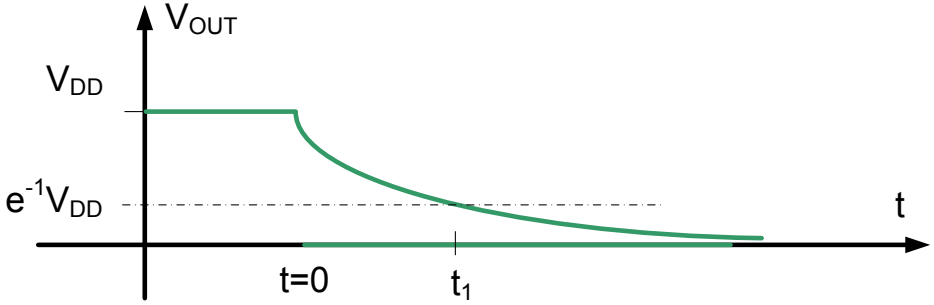
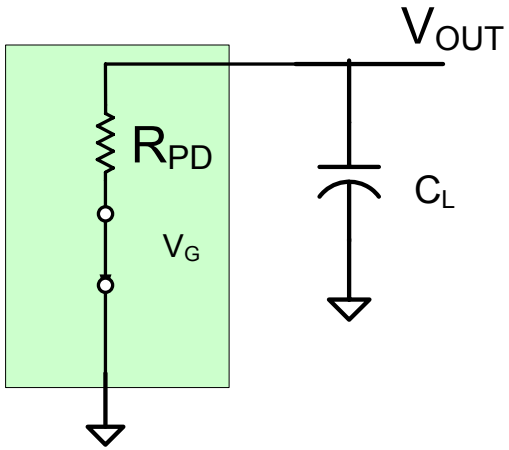




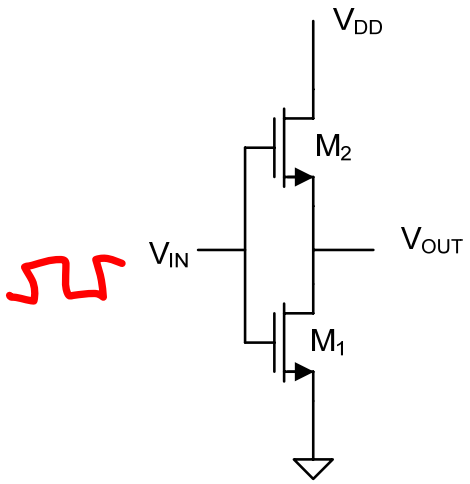


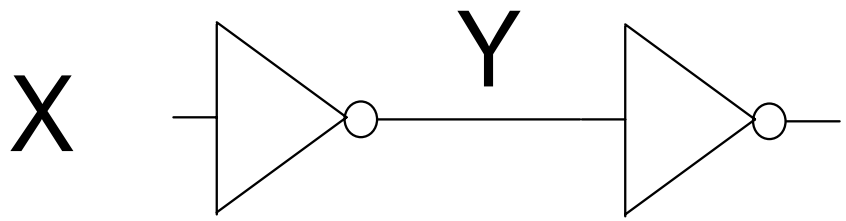


$$t_{HL} \cong R_{PD} C_L$$

$$t_{LH} \cong R_{PU} C_L$$

Propagation Delay in Static CMOS Family



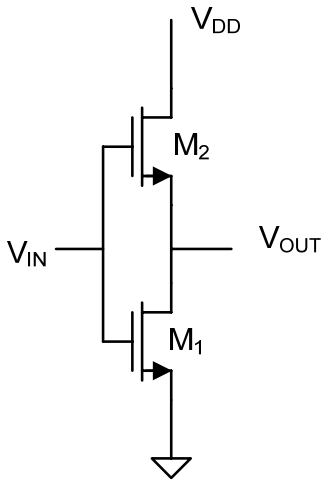


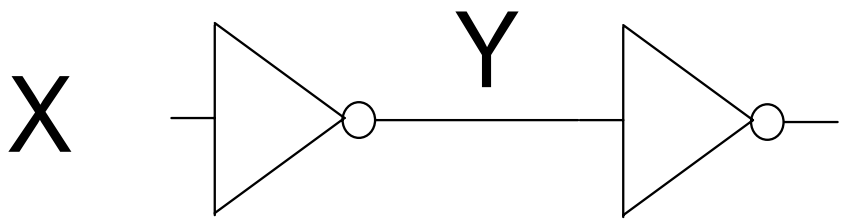
$t_{HL} \simeq (2.5\,k)(2\,fF) = 5\,psec$

$t_{LH} \simeq (7.5\,k)(2\,fF) = 15\,psec$

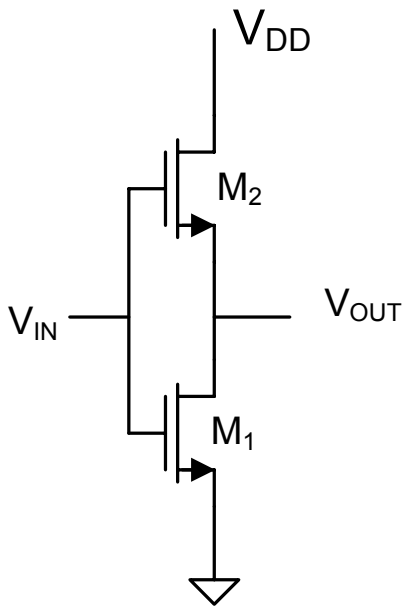
$T_{clock} \simeq t_{HL} + t_{LH} \simeq 20\,psec \sim 50\,GHz$

Propagation Delay in Static CMOS Family





Device Sizing

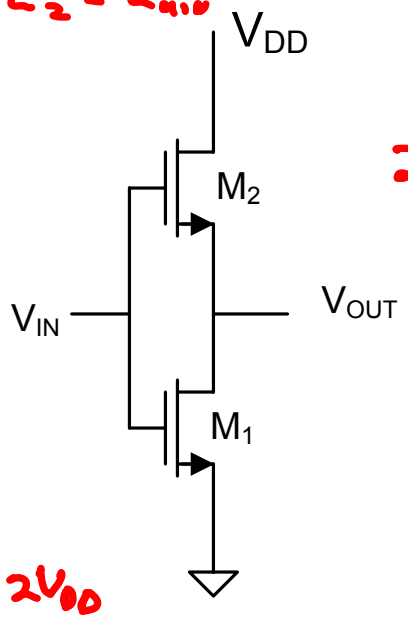


- Since not ratio logic, V_H and V_L are independent of device sizes for this inverter
- With $L_1=L_2=L_{min}$, there are 2 degrees of freedom (W_1 and W_2)

Sizing Strategies

- Minimum Size
- Fixed V_{TRIP}
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance

Device Sizing



- Minimum Size

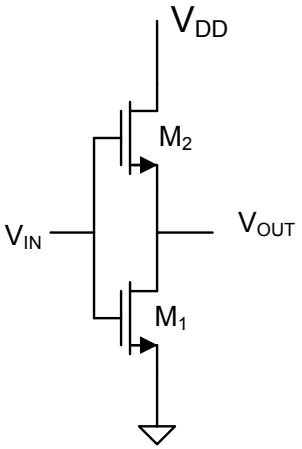
$W_1=W_2=W_{MIN}$

also provides minimum input capacitance

- t_{LH} is longer than t_{HL}

$$V_{IN_{TRIP}} = \frac{(0.2V_{DD}) + (V_{DD} - 0.2V_{DD})\sqrt{\frac{1}{3}}}{1+\sqrt{\frac{1}{3}}} = .42V_{DD}$$

Device Sizing



Equal Rise-Fall Times

$$\frac{t_{LH}}{t_{HL}} = \frac{R_{PU}C_{OX}}{R_{PD}C_{OX}} = \frac{\mu_n}{\mu_p}$$

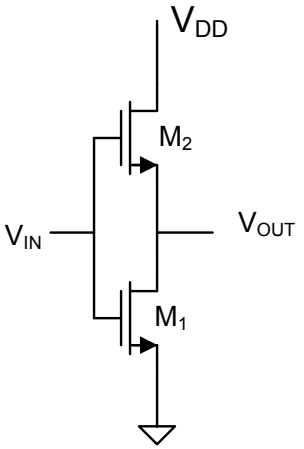
Thus if $t_{HL}=t_{LH}$, must have

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

What about the second degree of freedom?

V_{TRIP}=?

Device Sizing



Equal Rise-Fall Times

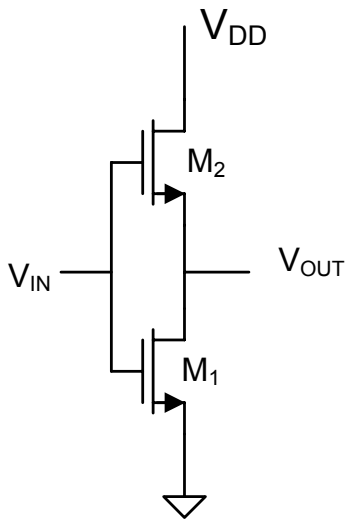
$$\frac{t_{LH}}{t_{HL}} = \frac{R_{PU}C_{OX}}{R_{PD}C_{OX}} = \frac{\mu_p}{\mu_n}$$

Thus if $t_{HL}=t_{LH}$, must have

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p}$$

$$V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}$$

Device Sizing



Fixed V_{TRIP}

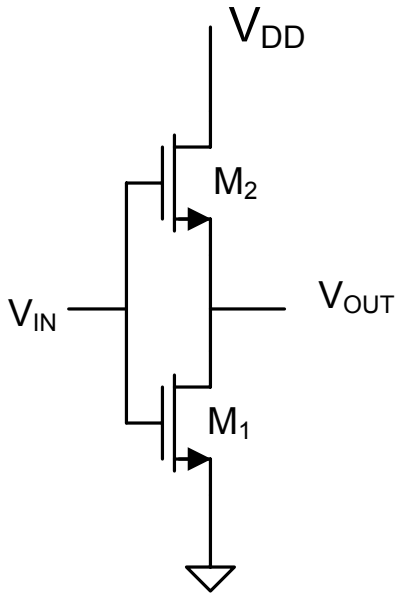
Set $V_{TRIP}=V_{DD}/2$

$$\frac{(.2V_{DD})+(V_{DD}-.2V_{DD})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}=\frac{V_{DD}}{2}$$

$W_1 = W_{min}$
$W_2 = 3 W_{min}$

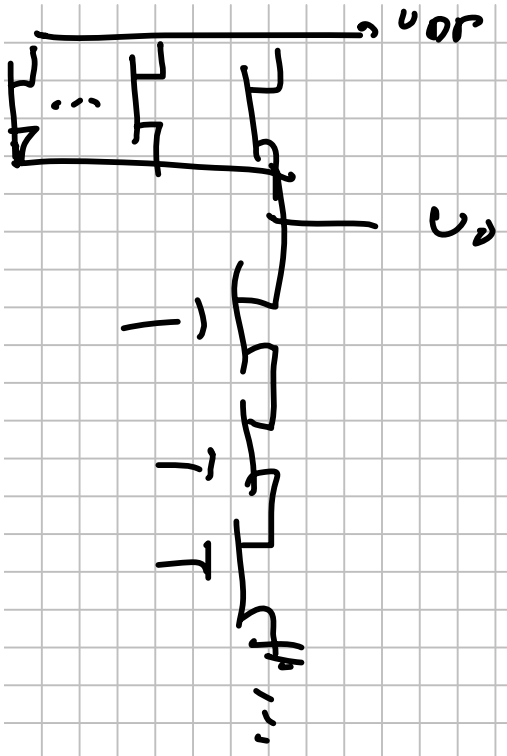
Solving, obtain $W_2/W_1=\mu_n/\mu_p$

Device Sizing



Sizing Strategies

- Minimum Size
- Fixed V_{TRIP} = $\frac{V_{DD}}{2}$
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance



for min sized

$t_{HL} = k R_{pd} C_L = k t_{HL\,Ref}$, $t_{LH} = 3 R_{pd}$

$FI = 2 C_{ox} W_{min} L_{min} = \frac{C_{REF}}{2}$

---

for equal worst-case rise & fall

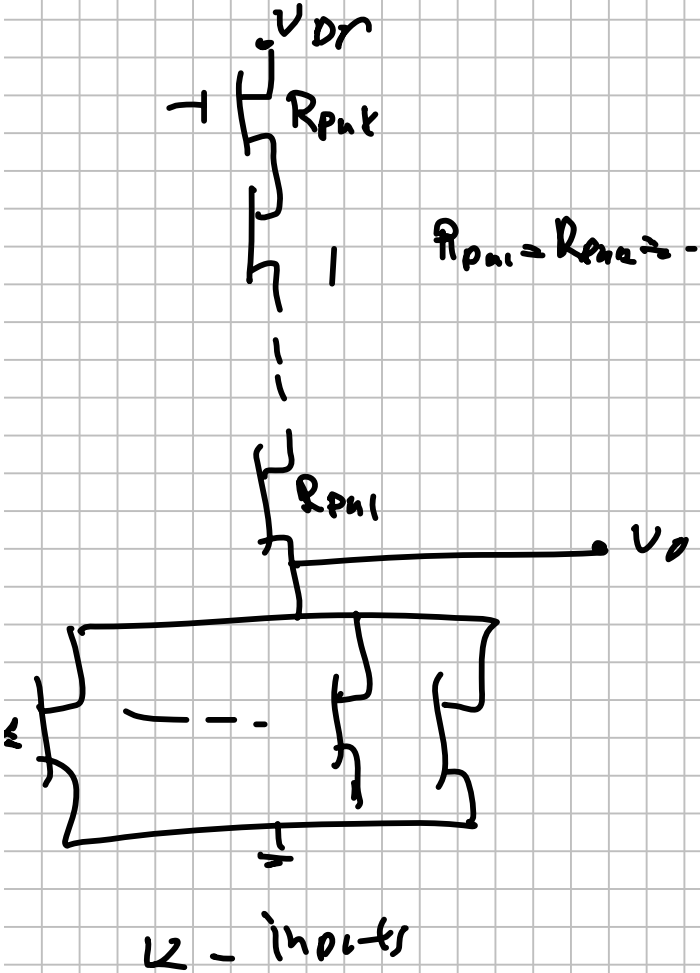
$W_n = (W_{min})\, k$

$W_p = 3 W_{min}$

~~FI~~ $FI = C_{ox} k W_{min} L_{min} + 3 C_{ox} W_{min} L_{min}$

$= (3+k) C_{ox} W_{min} L_{min}$

$= \frac{3+k}{4} C_{REF}$



- Equal worst case rise & fall times
- Set equal to that of an Inverter with equal rise & fall times

$R_{pu1} = R_{pu2} = \dots = R_{puk} = R_{pu}$

$t_{HL} =$ { $R_{pd} C_L$; $\frac{R_{pd}}{2} C_L$; $\vdots$; $\frac{R_{pd}}{k} C_L$ }

"worst" is longest

$R_{pd} = R_{pd_{REF}}$

$t_{LH} = k R_{pu} C_L = R_{pd} C_L$

$R_{pu} = \frac{R_{pd}}{k}$

$R_{pu} = \frac{\mu_n}{\mu_p} R_{pd} \Rightarrow \frac{\mu_n}{\mu_p} W_p = \frac{\mu_n}{\mu_p} k$

$\simeq 3k$

$C_{in_{REF}} = 4 C_{ox} W_{min} L_{min}$

$Fan\ in = \frac{3k+1}{4} C_{REF}$

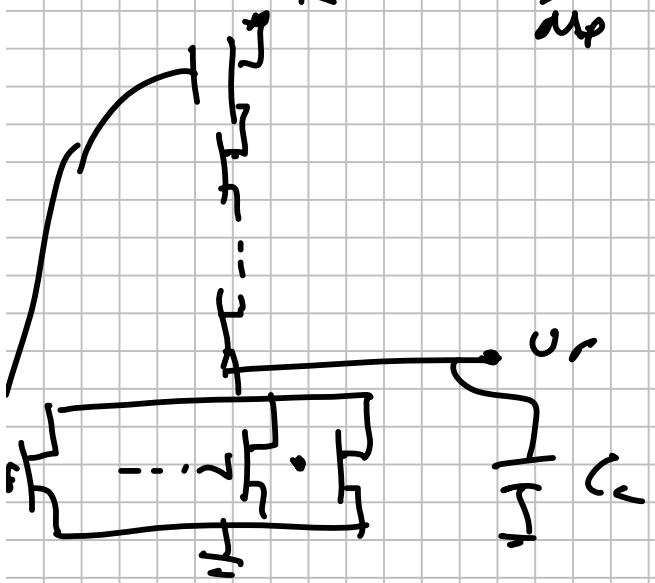
Fan in $(C_{ox} W_{min} 2nd_1 + C_{ox} W_{min} (nk) L_{min})$
$= (3k+1) C_{ox} W_{min} L_{min}$

To Inverter with $t_{HL} = t_{LH}$ & all devices as small as possible ($W_1 = W_{min}$, $W_2 = 3 W_{min}$, $L_1 = L_2 = L_{min}$) called Ref. Inverter

Sizing multiple-input gates

- minimum
- equal rise & fall (worst case)

$\frac{\mu_n}{\mu_p} = 3$



$L_1 = L_2 = L_{min}$

$W_1 = W_2 = W_{min}$

$$t_{HL} = \begin{cases} R_{pd} C_L & \text{for 1 input chg} \\ \frac{R_{pd}}{2} C_L & \text{for 2 inputs} \\ \vdots & \\ \frac{R_{pd}}{K} C_L & \text{for all K change} \end{cases}$$

Will trans only if all inputs are "1" prior to clock, 1, 2, .. -- K go high at clock

Worst case $R_{pd} C_L$

$$t_{LH} = K R_{pu} C_L = 3K R_{pd} C_L$$

Fan In on each input $= C_{ox} W_1 L_1 + C_{ox} W_2 L_2 = 2 C_{ox} W_{min} L_{min}$